

GaN 650V GaN HEMT RC65D270C

Description

The RC65D270C Series 650V, 270mΩ gallium nitride (GaN) FETs are normally-off devices.

RealChip GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and lower dynamic on-resistance, delivering significant advantages over traditional silicon (Si) devices.

RealChip is a leading-edge wide band gap supplier with world-class innovation .

Application

- Adapter
- Renewable energy
- Telecom and data-com
- Servo motors
- Industrial
- Automotive

General Features

Easy to drive—compatible with standard gate drivers

Low conduction and switching losses

RoHS compliant and Halogen-free

Benefits

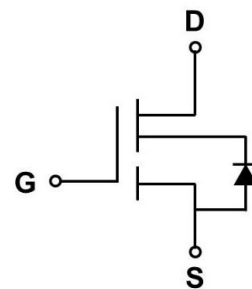
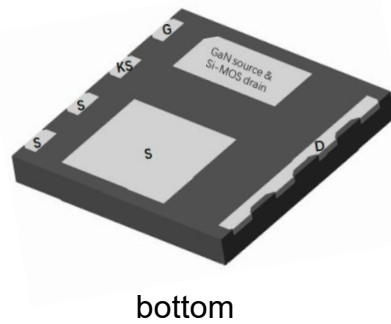
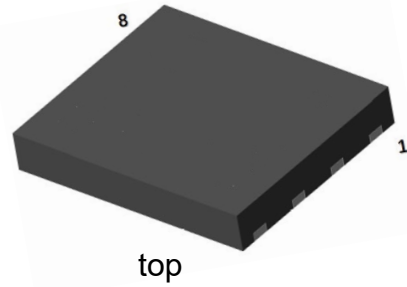
Increased efficiency through fast switching

Increased power density

Reduced system size and weight

Ordering Information

Part Number	Package	Package Configuration
RC65D270C	DFN 5*6	Source



Circuit Symbol

Features

BV_{DSS}	$R_{DS(on)}$	I_{DS}	Q_G
650V	270mΩ	9.3A	8.7nC

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Absolute Maximum Ratings

$T_c=25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Limit value	Unit	
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	650	V	
$V_{(TR)DSS}$	Drain to source voltage-transient ^a	800		
V_{GSS}	Gate to source voltage	-20~+20		
I_D	Continuous drain current @ $T_c=25^\circ\text{C}$ ^b	9.3	A	
	Continuous drain current @ $T_c=125^\circ\text{C}$ ^b	4.2		
I_{DM}	Pulse drain current (pulse width: 10 μs)	15	A	
P_D	Maximum power dissipation @ $T_c=25^\circ\text{C}$	56	W	
T_c	Operating temperature	Case	-55~150	$^\circ\text{C}$
T_J		Junction	-55~150	$^\circ\text{C}$
T_S	Storage temperature	-55~150	$^\circ\text{C}$	

a. In off-state, spike duty cycle $D<0.01$, spike duration $<1\mu\text{s}$

b. For increased stability at high current operation

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Thermal Resistance

Symbol	Parameter	Limit value	Unit
$R_{\theta JC}$	Junction-to-case	2.2	°C /W

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Electrical Parameters

$T_j=25^\circ\text{C}$ unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	-	-	V	$V_{GS}=0V$
$V_{GS(th)}$	Gate threshold voltage	3.3	3.9	4.5	V	$V_{DS}=1V, I_{DS}=1mA$
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	-	-7	-	mV/ $^\circ\text{C}$	
$R_{DS(on)}$	Drain-source on-Resistance	-	270	320	m Ω	$V_{GS}=10V, I_D=1A, T_J=25^\circ\text{C}$
		-	570	-		$V_{GS}=10V, I_D=1A, T_J=150^\circ\text{C}$
I_{DSS}	Drain-to-source leakage current	-	1	10	μA	$V_{DS}=650V, V_{GS}=0V, T_J=25^\circ\text{C}$
		-	5	100		$V_{DS}=650V, V_{GS}=0V, T_J=150^\circ\text{C}$
I_{GSS}	Gate-to-source forward leakage current	-	-	± 100	nA	$V_{GS}=\pm 20V$
C_{ISS}	Input capacitance	-	333	-	pF	$V_{GS}=0V, V_{DS}=400V, f=1MHz$
C_{OSS}	Output capacitance	-	18	-		
C_{RSS}	Reverse capacitance	-	3.7	-		
Q_G	Total gate charge	-	8.7	-	nC	$V_{DS}=400V, V_{GS}=0V \text{ to } 10V, I_D=1A$
Q_{GS}	Gate-source charge	-	2.2	-		
Q_{GD}	Gate-drain charge	-	2.6	-		
Q_{OSS}	Output charge	-	24	-	nC	$V_{GS}=0V, V_{DS}=0V \text{ to } 400V, f=1MHz$
$t_{D(on)}$	Turn-on delay	-	3.2	-	ns	$V_{DS}=400V, V_{GS}=0V \text{ to } 10V, I_D=2.1A,$ $R_{G-on(ext)}=6.8\Omega, R_{G-off(ext)}=2.2\Omega,$ $L=250\mu\text{H}$
t_R	Rise time	-	5.5	-		
$t_{D(off)}$	Turn-off delay	-	7.4	-		
t_F	Fall time	-	27	-		

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Electrical Parameters

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Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
V_{SD}	Source-Drain reverse voltage	-	2.5	-	V	$V_{GS}=0\text{V}$, $I_{SD}=10\text{A}$
t_{RR}	Reverse recovery time	-	14	-	ns	$I_F=5\text{A}$, $V_{DD}=400\text{V}$, $dI_F/dt=165\text{A}/\mu\text{s}$
Q_{RR}	Reverse recovery charge	-	6.5	-	nC	

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Typical Characteristics

$T_j=25^\circ\text{C}$ unless otherwise stated

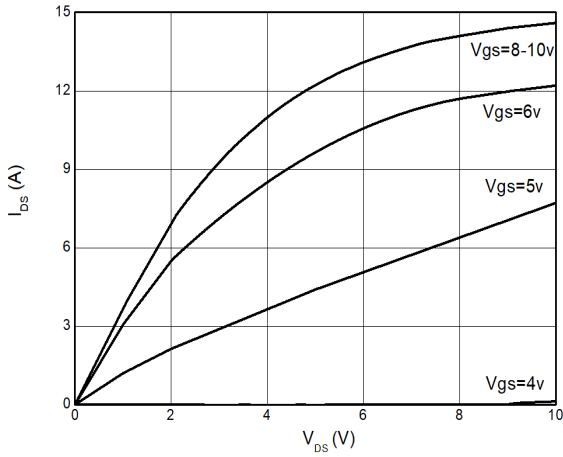


Figure 1. Typical Output Characteristics $T_j=25^\circ\text{C}$

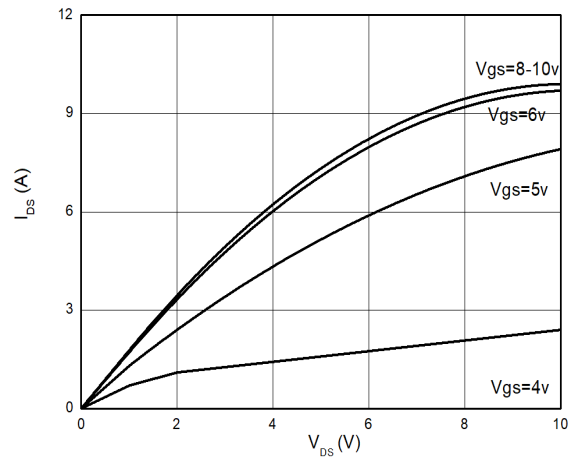


Figure 2. Typical Output Characteristics $T_j=125^\circ\text{C}$

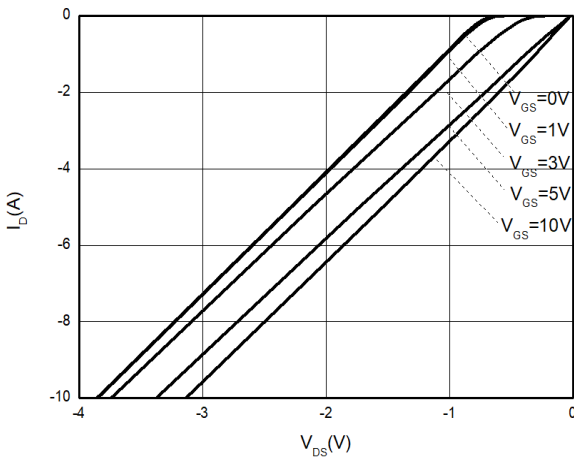


Figure 3. Channel Reverse Characteristics $T_j=25^\circ\text{C}$

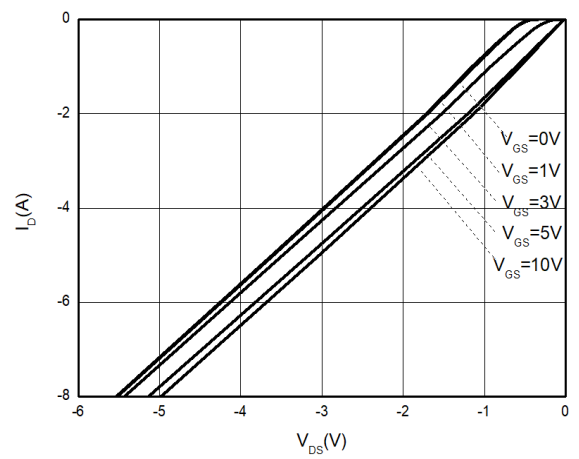


Figure 4. Channel Reverse Characteristics $T_j=125^\circ\text{C}$

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Typical Characteristics

$T_j=25^\circ\text{C}$ unless otherwise stated

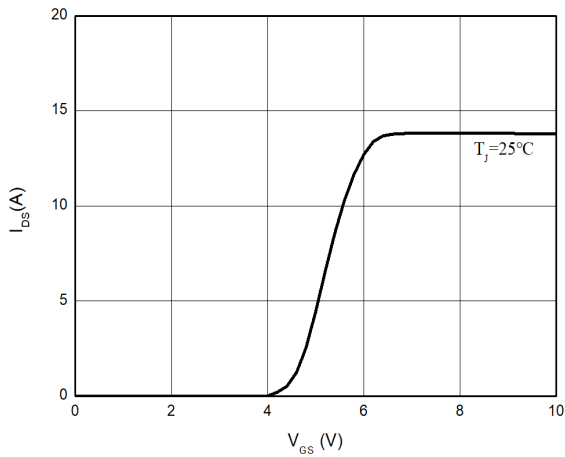


Figure 5. Typical Transfer Characteristics ($V_{DS}=10\text{V}$)

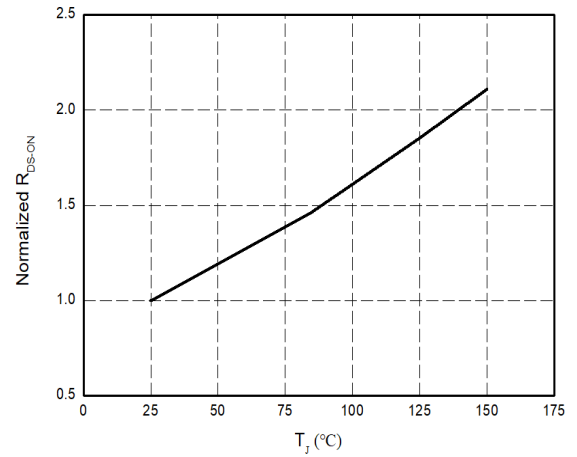


Figure 6. Normalized On-resistance

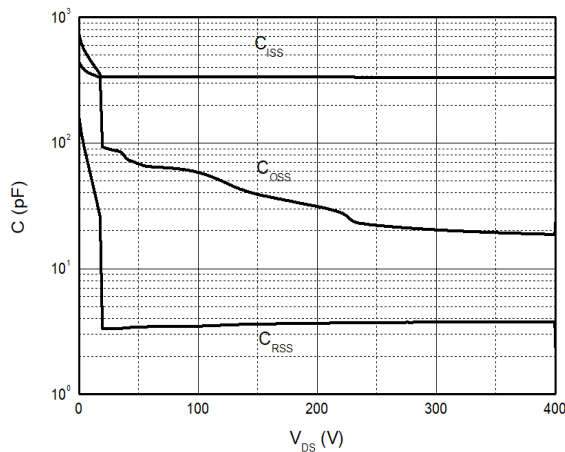


Figure 7. Typical Capacitance ($f=1\text{MHz}$)

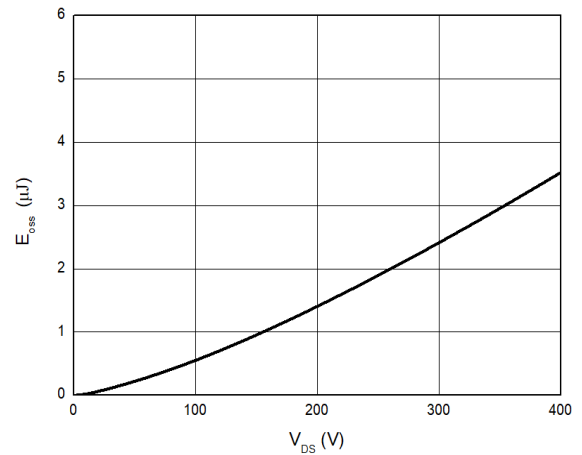


Figure 8. Typical C_{OSS} Stored Energy

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Typical Characteristics

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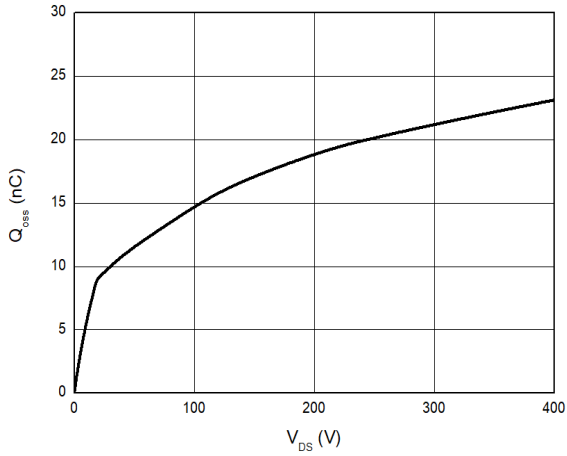


Figure 9. Typical Q_{oss}

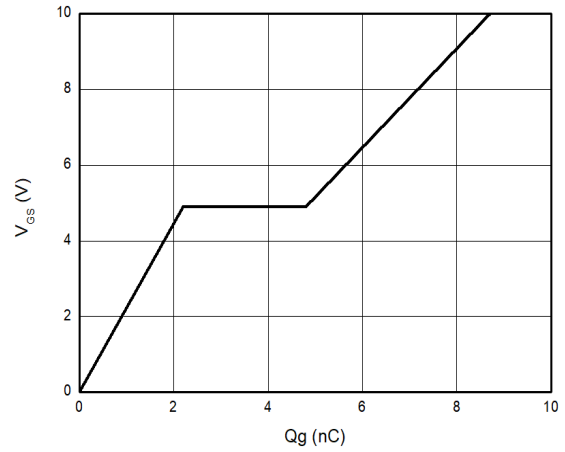


Figure 10. Typical Gate Charge ($V_{DS}=400\text{V}$, $I_D=1\text{A}$)

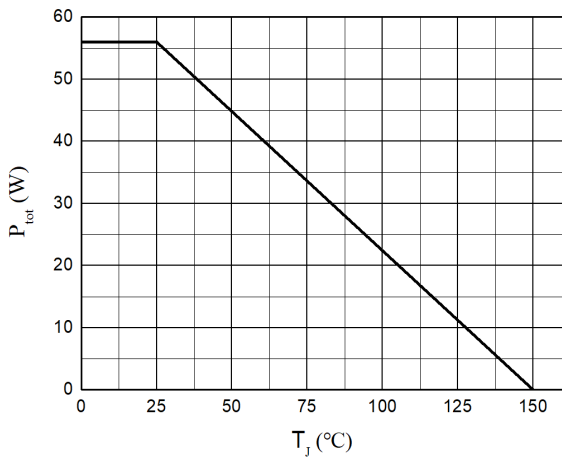


Figure 11. Power Dissipation

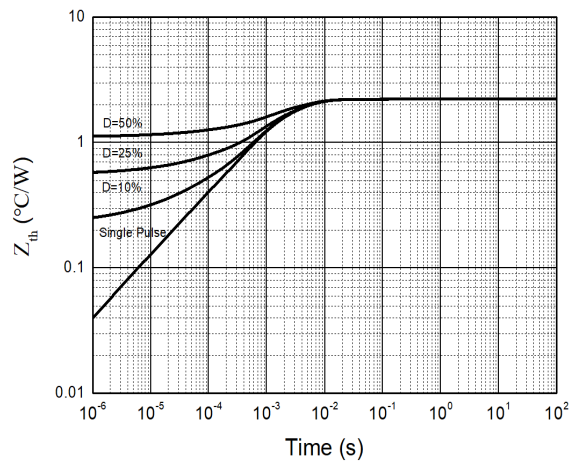


Figure 12. Transient Thermal Resistance

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Typical Characteristics

$T_J=25^\circ\text{C}$ unless otherwise stated

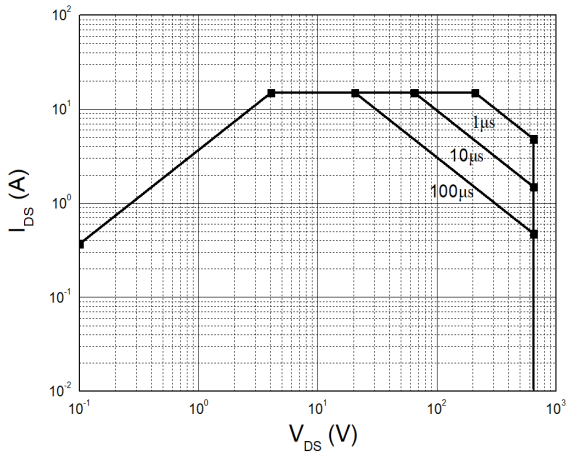


Figure 13. Safe Operating Area $T_J=25^\circ\text{C}$

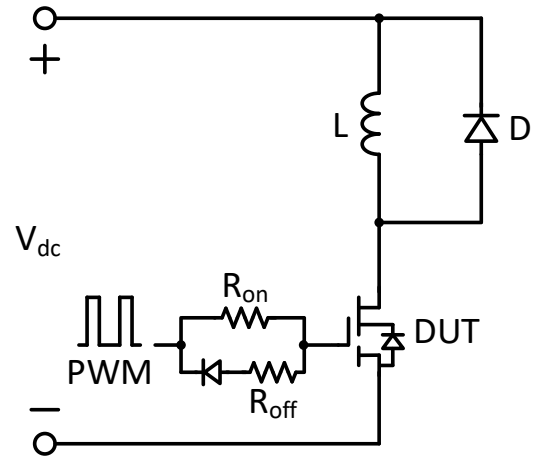


Figure 14. Switching times with inductive load

$V_{DS}=400\text{V}$, $V_{GS}=0\text{V to }10\text{V}$, $I_D=2.1\text{A}$,
 $R_{G-on(ext)}=6.8\Omega$, $R_{G-off(ext)}=2.2\Omega$, $L=250\mu\text{H}$

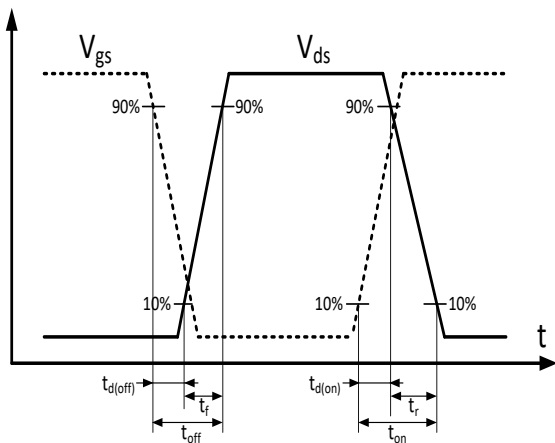


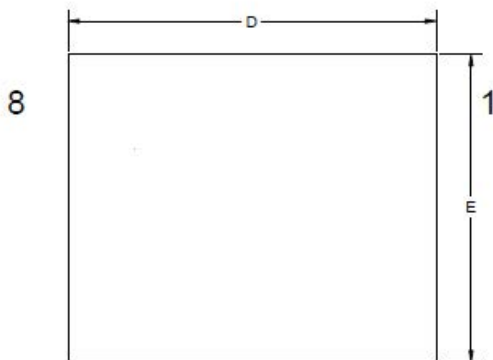
Figure 15. Switching times with waveform

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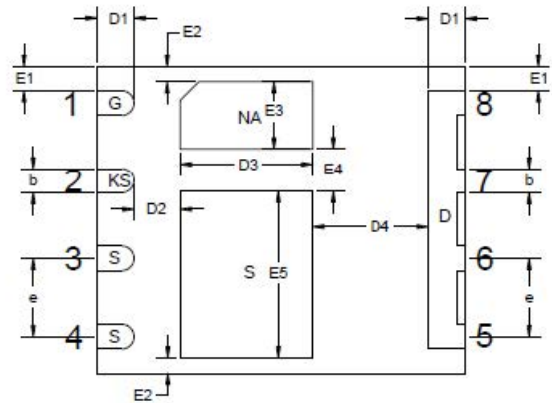
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PACKAGE DIMENSIONS

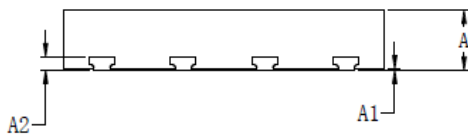
TOP VIEW



BOTTOM VIEW



Side View(left/right)



Symbol	Min. (mm)	Mean. (mm)	Max. (mm)
A	0.850	0.900	0.950
A1	0.000	0.020	0.050
A2	0.203REF		
D	5.900	6.000	6.100
E	4.900	5.000	5.100
D1	0.500	0.600	0.700
D2	0.650	0.750	0.850
D3	2.050	2.150	2.250
D4	1.800	1.900	2.000
E1	0.295	0.395	0.495
E2	0.195	0.295	0.395
E3	0.990	1.090	1.190
E4	0.600	0.700	0.800
E5	2.610	2.710	2.810
b	0.300	0.400	0.500
e	1.170	1.270	1.370